

1 Please amend Claim 17 as follows.

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3 17. (Currently Amended) The data processing unit as  
4 recited in claim 13 ~~wherein~~ wherein the UTOPIA ATM URDATA  
5 signal corresponds to an I/O OUTDATAVALID signal, and  
6 wherein a UTOPIA ATM UXCLAV signal corresponds to an I/O  
7 INDATAVALID signal.

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13 **Remarks**

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15 Claims 1-17 have been presented for examination in the  
16 above identified U.S. Patent Application.

17

18 Claims 1-17 have been rejected in the above-identified  
19 Office Action.

20

21 Claims 1-3, 7, 8, 11-14, 16 and 17 have been amended  
22 by this Amendment A.

23

24 Claims 1-17 are still in the Application and  
25 reconsideration of the application is hereby respectfully  
26 requested.

27

28 Referring to Paragraph 1 of the Office Action, the  
29 disclosure has been objected to because of cited  
30 informalities. With respect to items (a), (b) (c) and (d),

1 the informality has been amended by this Amendment A.  
2 Therefore, objection to the disclosure for the reasons  
3 cited by Examiner has been answered by amendment.  
4

5 Referring to Paragraph 2 of the Office Action, Claims  
6 12 and 17 have been objected to because of informalities  
7 kindly pointed out by Examiner. The cited informalities  
8 have been corrected by this Amendment A. Therefore,  
9 objection to Claims 12 and 17 have been answered by  
10 amendment.  
11

12 Referring to Paragraph 3 of the Office Action, Claims  
13 1-3,5-8 and 10 have been rejected under 35 U.S.C. 102(b)  
14 as being anticipated by U.S. Patent 5,625,625 issued in the  
15 name of Oskouy et al (hereinafter referred to as Oskouy).  
16 Referring to Paragraph 4, claims 4 and 11-17 have been  
17 rejected under 35 U.S.C. 103(a) as being unpatentable over  
18 Oskouy (cited above) in view of U.S. Patent 6,732,206  
19 issued in the name of Jensen et al (herein after referred  
20 to as Jensen). Referring to Paragraph 9 of the Office  
21 Action, Claim 9 has been rejected under 35 U.S.C. 103(a) as  
22 being unpatentable over Oskouy (cited above).  
23

24 Before discussing the relationship of the references  
25 to the invention sought to be protected, a brief discussion  
26 of the invention is herewith provided. In modern  
27 microprocessing systems, a general purpose microprocessor  
28 is provided along with at least one digital signal  
29 processor. The digital signal processor typically performs  
30 computation-intensive calculations under the command of the

1 general purpose microprocessor. The communication can take  
2 several forms, either an I/O protocol or a UTOPIA protocol.

3  
4 In addition, the central processing unit, whether a  
5 microprocessor or digital signal processor, is currently  
6 designed to operate in combination with a direct memory  
7 access unit. The direct memory access unit off-loads  
8 several memory operations thereby relieving the coupled  
9 processor of essentially routine operations. However, for  
10 a variety of reasons, the UTOPIA protocol was adopted. The  
11 signals with the Utopia protocol could not be directly  
12 applied to the direct memory access unit. In addition, the  
13 processor/direct memory access combination was complex  
14 enough so that once the combination circuit was debugged  
15 and design deemed appropriate for use in circuit  
16 fabrication, any redesign involving the direct memory  
17 access unit was undesirable.

18  
19 Instead of a redesign, the present invention provides  
20 an interface between the direct memory access unit and the  
21 communication bus that can transmit both UTOPIA protocol  
22 signals and I/O protocol signals. This interface unit is  
23 relatively simple and can be added to the circuit board  
24 without redesign of the direct memory access unit/processor  
25 combination.

26  
27 In order to clarify the invention sought to be  
28 protected by the Claims, Claims 1, 7, and 11, the  
29 independent Claims of the Application, have been amended to  
30 include explicitly the direct memory access unit as part of

1 the structure. This type of amendment is clearly supported  
2 by the Specification and by dependent Claims.

3

4 Referring to the Oskouy reference and the Jensen  
5 reference, neither of these references describes or  
6 suggests an interface unit mediating data flow between a  
7 bus and the direct memory access unit/processor  
8 combination. As pointed out above, the availability of the  
9 present interface unit to relieves the designer from the  
10 task of redesigning the direct memory access unit/processor  
11 combination. By retaining the original direct memory  
12 access unit/processor combination the interface unit can be  
13 relatively simple. Referring to the Oskouy and Jensen  
14 reference, these references appear to provide the data  
15 groups directly to the central processing unit requiring  
16 the central processing unit and associated apparatus to  
17 provide the processing required to transfer the data groups  
18 to appropriate location. Clearly, the presence of direct  
19 memory access unit is not a matter of design choice but  
20 permits a relatively simple interface to provide for the  
21 transfer of signal groups with two protocols. To emphasize  
22 this advantage, dependent Claims have been amended to  
23 provide a limitation of all of the apparatus being  
24 fabricated on a single chip. Therefore, rejection of the  
25 Claims by either Oskouy or Jensen is not appropriate.

26

27 Consequently, rejection of Claims 1-17 under 35 U.S.C.  
28 102(b) or under 35 U.S.C. 103(a) either over Oskouy alone  
29 or in combination with Jensen is respectfully traversed.

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